The Implementation of the ATLAS Level-1 Muon Trigger in the Barrel Region

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Introduction

The level-1 muon trigger of ATLAS in the barrel region is based on fast, finely segmented detectors to identify penetrating charged particles, pointing to the interaction region. The trigger is designed to unambigously identify the interaction bunch-crossing and to provide a sharp threshold over a large interval of transverse momentum. For the muon trigger system in the central toroid, Resistive Plate Chambers (RPC) are proposed for their good time resolution, easiness in the segmentation and low cost of production. The different momentum selection criteria required by the physics processes are met using a low and high Pt triggers.

The trigger logic is done with a dedicated coincidence matrix circuit, based on an ASIC, already developed in 0.5 micron CMOS technology, within the RD27 collaboration of CERN. The X-Y inputs to the coincidence matrix are given by the discriminated and shaped signals from the RPC of different planes.

The trigger system is subdivided into 48 sectors and in order to minimize the cable length and the trigger latency the coincidence matrices will be distributed along the apparatus. The information from the coincidence matrices of each sector will be collected by a local Sector Muon Trigger, located in the center of the detector. The output of the sectors will be sent via optical links to the Central Muon Trigger that generates the global muon trigger information that is passed to the Level-1 Central Trigger Processor.

1 The trigger algorithm

The first level muon trigger is based on fast, finely segmented detectors. The intrinsic time resolution of the detectors should be smaller than the bunch crossing period. Given the configuration of the experiment, the trigger is divided in three different regions:

- the barrel detectors in the central toroid, $|\eta| < 1.1$;
- the end-cap detectors in the central toroid, $1.1 < |\eta| < 1.6$;
- the detectors in the end-cap toroids, $|\eta| > 1.6$.

To cope with the different levels of particle flux, we propose to use Resistive Plate Chambers [1] (RPC) in the barrel and Thin-Gap Wire Chambers [2] (TGC) in the end-cap. In both detectors the signal is read out on electrodes segmented in strips with an intrinsic time resolution of ≈ 2 ns (RPC) and ≈ 5 ns (TGC). The propagation time of the signal along the strips is kept below 10 ns.

The trigger is done with a fast coincidence between z-strips on different planes. The number of trigger planes is defined by the need to minimize the rate of accidental coincidences and to optimize the efficiency. The trigger detectors will also be used to provide the coordinate in the non-bending plane (r-ϕ) to the muon tracking system. This would allow to implement the trigger in two projections, r-z and r-ϕ. The trigger concept is outlined in Fig.1.

In the barrel we propose to use three trigger planes, two located close to the middle muon chambers and one located close to the external muon chambers. The middle planes are made of two RPC layers and the external plane is made of three RPC layers. The low p_T trigger requires a threefold majority coincidence of the four middle layers while the high p_T trigger requires a twofold majority coincidence of the three external layers and the low p_T.

The trigger logic is done with a dedicated coincidence matrix circuit based on a gate-array whose prototype was developed within the RD27 collaboration [3]. The x-y inputs to the coincidence matrix are given by the signals from the trigger planes. The transverse momentum threshold is defined by a "road" in the matrix and a trigger signal is generated when there is a valid coincidence within the road (Fig.2).

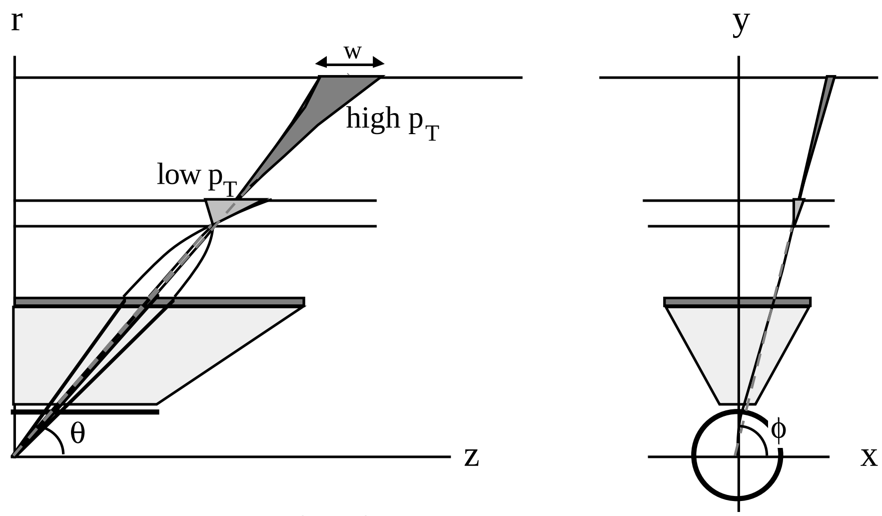


Fig.1 - Scheme of the first level muon trigger in the barrel

2 The coincidence matrix ASIC

A coincidence matrix demonstrator ASIC was developed by the DR27 collaboration [4]. The size of the matrix is 8 x 24 and the circuit can operate with two different thresholds symultaneously. To implement the low and high p_T triggers we use two ASICs. Fig.3 shows the basic cell of the matrix circuit and Fig.4 shows the way the coincidence matrices are connected to generate the trigger. For the low p_T trigger the inputs are the four middle layers and the logic is a 3/4 majority coincidence, while for the high p_T trigger the inputs are the three external layers and the confirmed output of the first matrix and the logic is a (2/3 majority coincidence) x (low p_T). To compensate for different propagation times of the signals from different detector layers, the delays of each group of *X* and *Y* inputs to the coincidence matrix can be adjusted inside the circuit with programmable micropipeline delays.

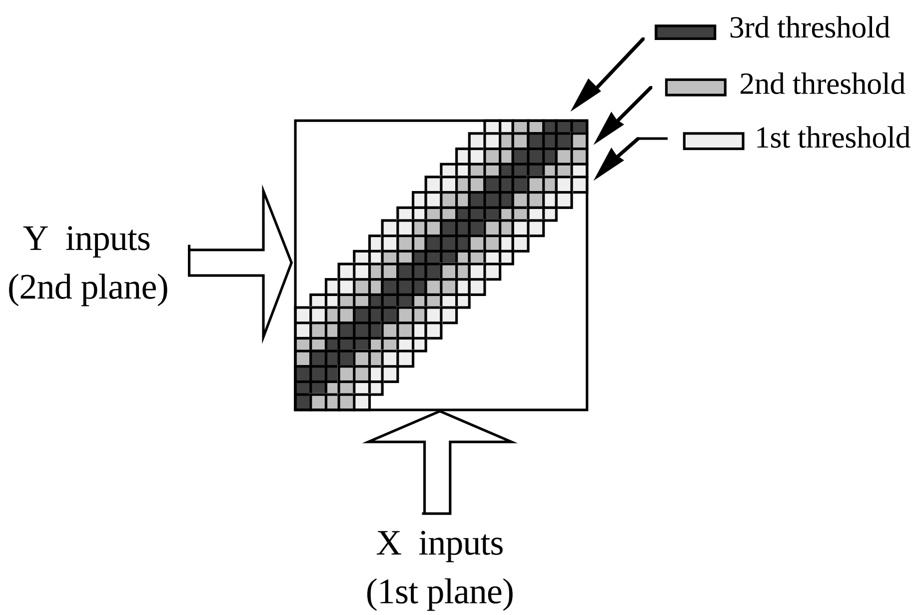
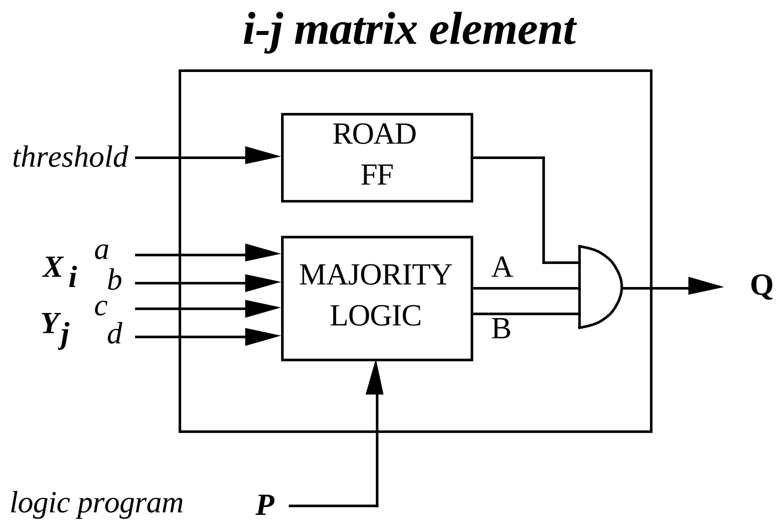


Fig.2 - The coincidence matrix

The coincidence matrix ASIC is developed using a gate-array from Fujitsu in 0.5 μm CMOS technology. The use of this technology allows an internal jitter of the circuit smaller than 2-3 ns and low power consumption.

The final design of the ASIC for the ATLAS first level muon trigger will be most probably developed in the same technology. The size of the matrix will probably be 32x48 and the circuit will operate with three different thresholds simultaneously.



P	*a*	*b*	*c*	*d*	A	B
LOW	$T_{1.1}$	$T_{1.2}$	$T_{2.1}$	$T_{2.2}$	3/4 of *abcd*	HIGH
HIGH	$T_{3.1}$	$T_{3.2}$	$T_{3.3}$	out low p_T	2/3 of *abc*	*d*

Fig.3 - Basic cell of the coincidence matrix

3 Bunch crossing identification and system synchronization

The time resolution of the first level trigger system should be smaller than the bunch crossing period of 25 ns. Thus it is mandatory to use very fast detectors and very precise timing circuits. A preliminary test has been done with the RD5 experimental set-up. In the test the outputs of two RPC planes were sent to a coincidence matrix built with very fast GaAs commercial components [5]. The measured time resolution was well below 25 ns [6].

The identification of the bunch crossing is done by latching the main clock with the coincidence matrix output. A x4 time interpolator (160 MHz) is used to tag the bunch crossing. For the synchronization of the system, we plan to make a logical subdivision of the muon trigger detectors in "timing zones" (Fig.5) such that the propagation time of the clock signal from one zone to the next one is equal to one bunch crossing period. The different zones will be synchronized by adding delays equal to integer numbers of the bunch crossing period. To compensate for the different times of flight of particles, additional programmable delays will be added to the clock signal to keep all coincidence matrices in phase.

In the barrel there are 24 ϕ sectors and each sector is segmented in about 20 coincidence matrices. Thus each coincidence matrix defines a RoI of $\Delta\phi \times \Delta\eta \approx 0.25 \times 0.10$. The output of the trigger will contain the information of the bunch crossing number, the p_T threshold and the RoI.

4 Lay-out of the trigger electronics

In order to minimize cable length and the trigger latency, the coincidence matrices will be distributed along the apparatus on printed boards attached to the external trigger detectors. The signals from the internal detector planes will be sent to the coincidence matrices via cables that introduce a delay slightly larger than the time of flight of particles. As said before this delay will be compensated in the coincidence matrix. The information from the coincidence matrices of each ϕ sector will be collected and elaborated by a local Sector Muon Trigger located on the detector. The outputs of the sector triggers will be sent via optical links to the Central Muon Trigger that generates the global muon trigger information that is passed to the Level-1 Central Trigger Processor. To minimize the cable length the two processors will be located in the same place.

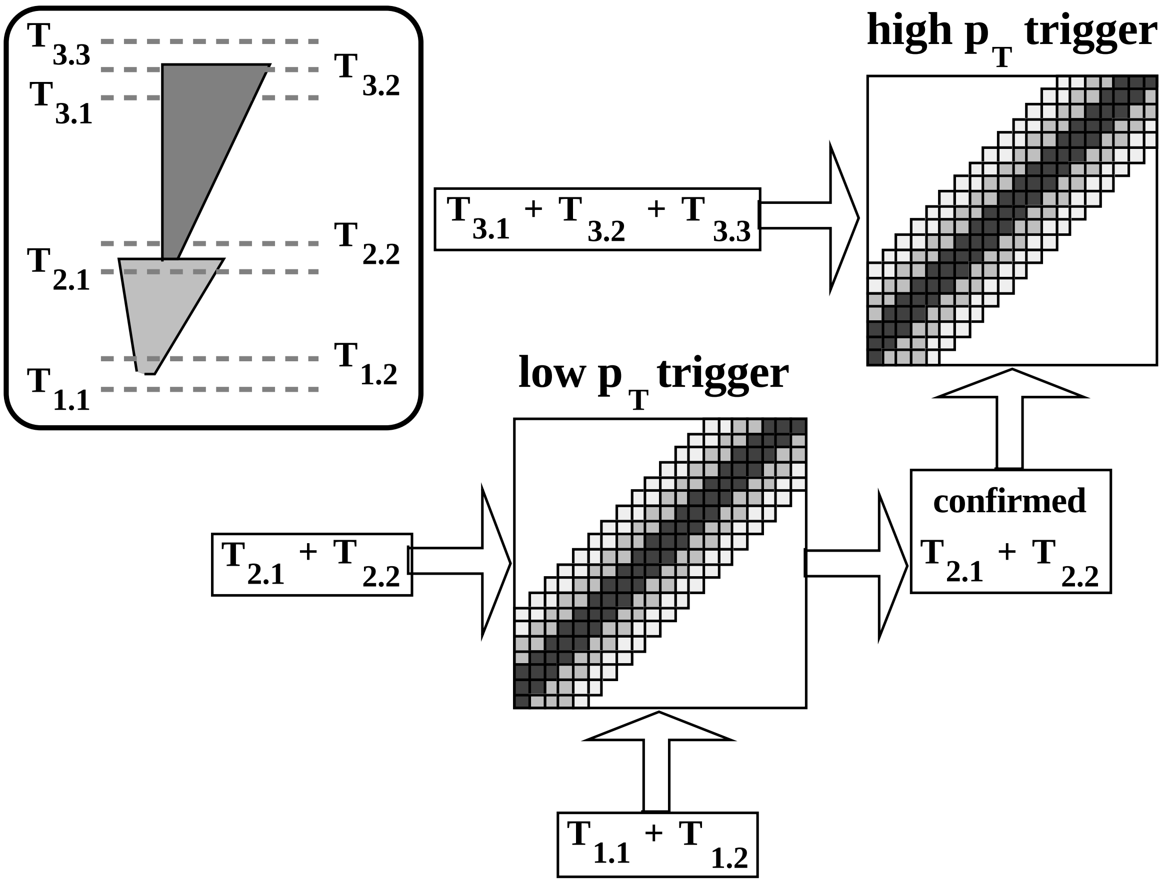


Fig.4 - Scheme of implementation of the low and high p_T muon trigger

5 Data Transmission

Each of the 48 local sector triggers generate a 32-bit word every 25 nsec. This is transmittet to the Central Muon Trigger over a pair of optical data link per sector:

number of tracks per sector (max 2)	(2 bits)
RoI for each track (4 bits)	(8 bits)
Pt range (2+2 bits from low and high Pt triggers)	(8 bits)
T0 counter (bunch crossing identification number)	(8 bits)
In reserve	(6 bits)

Otical links will connect the Sector Muon Trigger to the Central Muon Trigger. We plan to use optical links based on a GaAs transceiver chip whose prototype has been already developed and tested by INFN/Rome.

6 Trigger latency

We have evaluated the latency of the trigger system in the following way:

	ns	b.c.
particle time of flight	50	2
local logic (shaping time, signal propagation, coincidence matrix)	100	4
sector logic processing time	175	7

central logic processing time	175	7
cable delay (2 x 65 m)	650	26
	1150	46

As it can be seen from the table, the total delay is well below the goal of 2 μs foreseen for the ATLAS first level trigger latency.

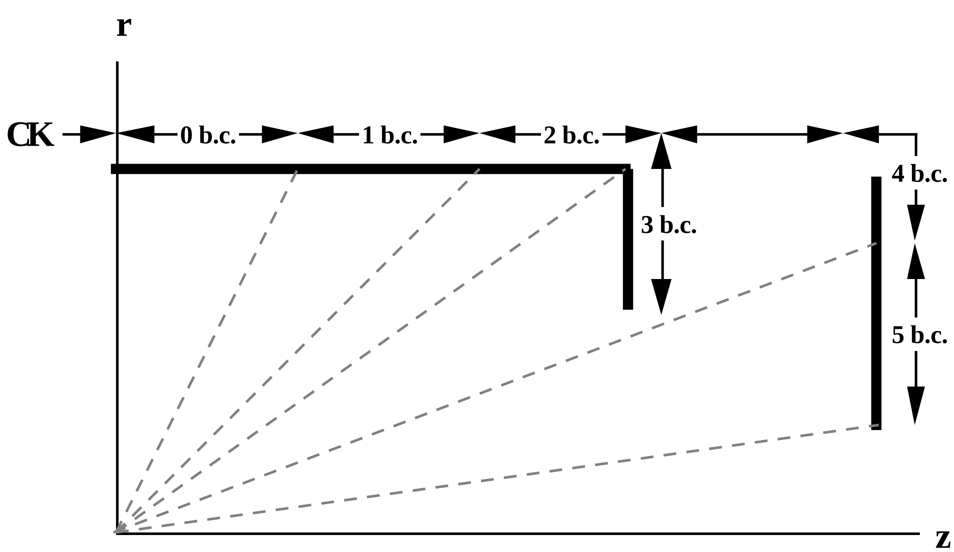


Fig.5 Timing zones of the distribution of the main clock

7 Timing

Timing is a critical issue in the muon trigger since the detectors extends over a very large area and the propagation time between different regions can be several bunch-crossing periods. Also the time of flight of particles in different regions can be of the same order of the bunch-crossing period.

The trigger system needs the distribution of the main clock over about 1000 points. Our project will make use of the Timing Control and Distribution System [7] developed in the framework of the RD-12 and RD-27 experiments. We have also considered the need for a timing calibration system to determine the correct settings for the programmable delays used in our bunch-crossing identification and system synchronisation and the possibility to generate artificial triggers for calibrating the electronics. In addition, we include time interpolators, synchronous with the main clock and running at four times its frequency. The value of the time interpolator provides a more precise timing of the trigger pulse within the bunch-crossing period. It will be possible to correct the timing of the trigger system by analysing the time interpolator data and by adjusting the programmable delays.

References

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